UNIT 5

DATA TRANSFER BTN MC’S USING ZIGBEE

ZIGBEE

- ZigBee communication is specially built for control and sensor networks on IEEE 802.15.4
- standard for wireless personal area networks (WPANs), and it is the product from ZigBee alliance. This communication standard defines physical and Media Access Control (MAC) layers to handle many devices at low-data rates.
- These ZigBee’s WPANs operate at 868 MHz, 902-928MHz, and 2.4 GHz frequencies. The data rate of 250 kbps is best suited for periodic as well as intermediate two-way transmission of data between sensors and controllers.

ADVANTAGES OF ZIGBEE

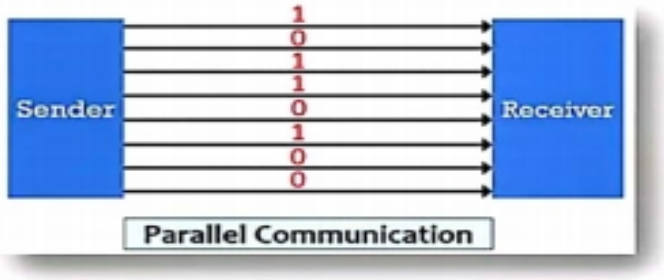
- ZigBee is a low-cost and low-powered mesh network widely deployed for controlling and monitoring applications where it covers 10-100 meters within the range.
- This communication system is less expensive and simpler than the other proprietary short-range wireless sensor Networks as Bluetooth and Wi-Fi
- ZigBee supports different network configurations for the master to master or master to slave communications

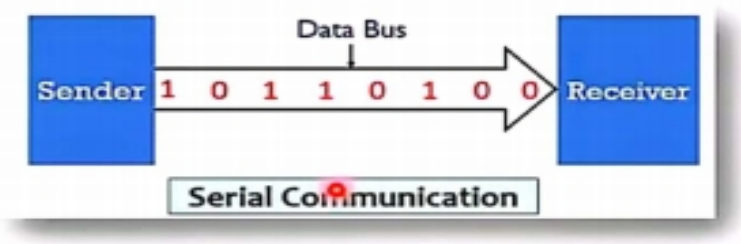
- . And also, it can be operated in different modes as a result the battery power is conserved. ZigBee networks are extendable with the use of routers and allow many nodes to interconnect with each other for building a wider area network.
- **How does ZigBee Technology Work?**

Parallel and serial data transfer

Parallel VS Serial Data Transfer

Sr.No	Parallel Data Transfer	Serial Data Transfer
1	Group of bits (8 bits) of data is transferred at a time	Only one bit of data transferred at a time
2	Data transfer rate is high.	Data transfer rate is low.
3	Preferred for short distance.	Preferred for long distance.
4	Cabling cost is more.	Cabling cost is less.
5	Less reliable.	More reliable.
6	Example: GPIB,PCI,ISA etc.	Example: RS232C, USB, HDLC etc.





Peripheral Control Registers(8051 Real Time Control)

PCON (Power Control)

- The PCON or Power Control register, as the name suggests is used to control the 8051 Microcontroller’s Power Modes and is located at 87H of the SFR Memory Space.
- Using two bits in the PCON Register, the microcontroller can be set to Idle Mode and Power Down Mode
- During Idle Mode, the Microcontroller will stop the Clock Signal to the ALU (CPU) but it is given to other peripherals like Timer, Serial, Interrupts, etc. In order to terminate the Idle Mode, you have to use an Interrupt or Hardware Reset.

PCON (Power Control)

- In the Power Down Mode, the oscillator will be stopped and the power will be reduced to 2V.
- To terminate the Power Down Mode, you have to use the Hardware Reset.
- Apart from these two, the PCON Register can also be used for few additional purposes.
- The SMOD Bit in the PCON Register is used to control the Baud Rate of the Serial Port.

PCON (Power Control)

- There are two general purpose Flag Bits in the PCON Register, which can be used by the programmer during execution.



SCON (Serial Control)

- SCON (Serial Control)
- The Serial Control or SCON SFR is used to control the 8051 Microcontroller’s Serial Port.
- It is located as an address of 98H.
- Using SCON, you can control the Operation Modes of the Serial Port, Baud Rate of the Serial Port and Send or Receive Data using Serial Port.
- SCON Register also consists of bits that are automatically SET when a byte of data is transmitted or received.

SCON (Serial Control)



SCON (Serial Control)

- SCON Register also consists of bits that are automatically SET when a byte of data is transmitted or received.

TCON (Timer Control)

- Timer Control or TCON Register is used to start or stop the Timers of 8051 Microcontroller. It
- also contains bits to indicate if the Timers has overflowed. The TCON SFR also consists of Interrupt related bits.



TMOD (Timer Mode)

- The TMOD or Timer Mode register or SFR is used to set the Operating Modes of the Timers T0 and T1. The lower four bits are used to configure Timer0 and the higher four bits are used to configure Timer1.

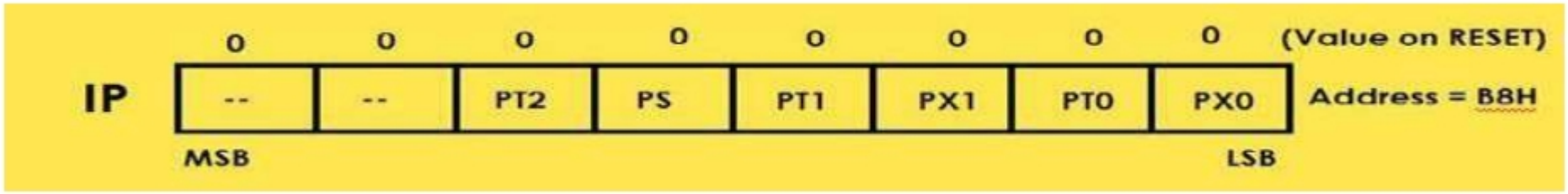


TMOD (Timer Mode)

- The Gatex bit is used to operate the Timerx with respect to the INTx pin or regardless of the
- INTx pin.
- GATE1 = 1 ==> Timer1 is operated only if INT1 is SET.
- GATE1 = 0 ==> Timer1 is operates irrespective of INT1 pin.
- GATE0 = 1 ==> Timer0 is operated only if INT0 is SET.
- GATE0 = 0 ==> Timer0 is operates irrespective of INT0 pin.
- The C/Tx bit is used selects the source of pulses for the Timer to count.
- C/T1 = 1 ==> Timer1 counts pulses from Pin T1 (P3.5) (Counter Mode)
- C/T1 = 0 ==> Timer1 counts pulses from internal oscillator (Timer Mode)

IP (Interrupt Priority)

- The IP or Interrupt Priority Register is used to set the priority of the interrupt as High or Low.
- If a bit is CLEARED, the corresponding interrupt is assigned low priority and if the bit is SET, the interrupt is assigned high priority.



Peripheral Data Registers
SBUF (Serial Data Buffer)

- The Serial Buffer or SBUF register is used to hold the serial data while transmission or reception.



ARM processor

- An ARM processor is one of a family of CPUs based on the RISC (reduced instruction set computer) architecture developed by Advanced RISC Machines (ARM)ARM makes 32-bit and 64-bit RISC multi-core processors.
- RISC processors are designed to perform a smaller number of types of computer instructions so that they can operate at a higher speed, performing more millions of instructions per second (MIPS).
- By stripping out unneeded instructions and optimizing pathways, RISC processors provide outstanding performance at a fraction of the power demand of CISC (complex instruction set computing) devices.

ARM processor

- ARM processors are extensively used in consumer electronic devices such as smartphones, tablets, multimedia players and other mobile devices, such as wearables.
- Because of their reduced instruction set, they require fewer transistors, which enables a smaller die size for the integrated circuitry (IC).
- The ARM processor’s smaller size, reduced complexity and lower power consumption makes them suitable for increasingly miniaturized devices

ARM processor

ARM processor features include:

- Load/store architecture.
- An orthogonal instruction set.
- Mostly single-cycle execution.
- Enhanced power-saving design.
- 64 and 32-bit execution states for scalable high performance.
- Hardware virtualization support.

ARM processor

- The simplified design of ARM processors enables more efficient multi-core processing and easier coding for developers.
- While they don't have the same raw compute throughput as the products of x86 market leader Intel, ARM processors sometimes exceed the performance of Intel processors for applications that exist on both architectures.